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Analysis of flip flop design using nanoelectronic single electron transistor

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Abstract

Single Electron Transistor (SET) is a nanoelectronic device that operates under the controlled mode of tunnelled individual electrons. In this paper, a comparative analysis was performed employing SET based D-Flip flop with conventional logic D-flip flop. SET is eminent nanoscale devices that have low power dissipation, high speed and performance. The flip flop design was simulated using SIMON simulator and the stability of its operation was analysed applying the Monte-Carlo method that represented stability with low power dissipation and matched the functionality of traditional CMOS devices.

Keywords: Logic Circuits, Coulomb Blockage, Nanoelectronics, Single Electron Device (SED), flip-flop.
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1. Introduction

The advancement of CMOS technology is still in back evolution and the increase in power utilization has become a main issue in the fabrication of large-scale integrated circuits. Consequently, the single-electron transistor (SET) has intriguedconsiderable attention because of its low power disbursement and high packing concentration. The information in the form of bits is represented by the presence or absence of single electrons at the quantum conducting islands. The fundamental principle of single-electronics is the Coulomb blockade was first observed and studied by Gorter [1].

It is widely known the size and transistor compactness facilitate vast improvement in the semiconductor based technology. Single-electron tunneling device [2] also has smart features like excellent current control, reduced dimensions and low noise behavior. These features should allow the realization of chips containing a number of the devices orders of magnitude greater than those indicated by the roadmap but still respecting the roadmaps area and power restrictions [3]. A variety of useful devices and concepts utilizing the single-electron tunneling features, such as, cellular automata, the binary decision device [4], and SET logic gates ie. OR, AND, NAND, NOR, etc. [5,6], single electron memories [7], control–control-Not gate [8], analog to digital converter [9], stochastic associative memory [10] have been projected and experienced by actual devices.

The need for computer-aided design and simulation of single-electron circuits has long been recognized. Several simulators and simulation methods have been developed to support single-electron circuit design. SIMON is such a simulator developed by Wasshuber et al [11].Fabrication of SEDs is an expensive and time-consuming process and, because of that, computer-aided design and simulation tools have been developed in order to study these circuits. A major improvement in SED circuits was achieved by the development of SIMON, which is a Monte Carlo-based tool capable to design, simulate and study SEDs and circuits.Up to date, SIMON has been used for various relevant studies and showed it is a proven tool for such a mission [12].

2. Single-Electron Tunnelling

2.1 Coulomb blockade

Single-electron circuits consist of conducting quantum islands, tunnel junctions, capacitors, and voltage source. The quantum islands are subjectively connected between the tunnel junctions, capacitors and voltage sources. The movement of single electron charge through the tunnel junction is referred as tunnelling, where the electrons are tunnelled through a tunnel junction strictly one after another. This tunnel event of an electron is described by single electronics orthodox theory also a stochastic nature and the energy quantization is in discrete process. If the additional electrons are injected through the energy barrier of the insulating layer, it may prevent the system is said to be Coulomb blockade.

The basic principle of single electronics is that one needs coulomb energy E_C to charge an island with an electron. This energy is:

$$E_C = e^2/2C >> 2k_BT \quad (1)$$

Where C_i C is the capacitance of the island, e is the elementary charge, k_B is Boltzmann's constant and T is the absolute temperature [13]. Since the electric charge flows through the tunnel junctions in multiples of electrons. To assure that electron states are localized on islands all tunnel resistances must be larger than the fundamental quantum resistance

$$R_T > R_Q = h/ e^2 \approx 25.813\ K\Omega \quad (2)$$

Where h is Planck's constant.

To simulate in a single-electron circuit the tunnel event of electrons from island to island has to determine the rates of all possible tunnel events due to free energy changes. The free energy F, of a single-electron circuit is the differences of the electrostatic energy U, stored in its capacitances and the work accomplished by the voltage sources of the single electron circuit W,

$$F = U - W \quad (3)$$

The electrostatic energy is given by

$$U = \frac{1}{2}(q, v)\left(\frac{V}{Q}\right) \quad (4)$$

Where q and v are the unknown variables of the island charge and voltage matrices respectively, and Q and V are the known variables of the island charge and voltage matrices, respectively. The work achieved by the voltage sources is given by

$$W = \sum \int V_n(t) i_n(t) dt \quad (5)$$

Where $V_n(t)$ t) is the voltage of the n^{th} voltage source and $i_n(t)$ t) is the current through the n^{th} voltage source. The tunnel rate Γ for a particular tunnel event is given by

$$\Gamma = \frac{\Delta F}{e^2 R_r\left[1-\exp\left(-\frac{\Delta F}{kT}\right)\right]} \quad (6)$$

Where ΔF is the free energy change due to this tunnelling event, R_T is the tunnel resistance on the electron transported through tunnel junction, and k_BT is the thermal energy. Overall tunnel rates for all possible tunnel events is determined using a Monte Carlo method combined with an exponential distribution of tunnel events The time duration of a particular event is given by

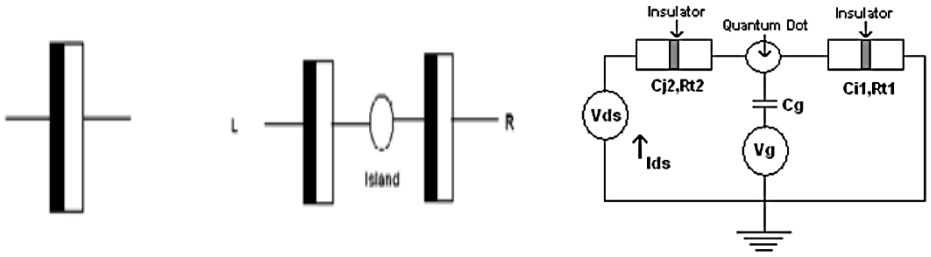
$$\Delta t = -\frac{In(r)}{r} \quad (7)$$

2.2 Monte Carlo Technique

Currently, two simulation approaches used in SET circuits. One is based on a Monte Carlo method, and the other on a Master equation Method. The Monte Carlo approach starts with all possible tunnel events, considered to be independent and exponentially distributed. Calculates their probabilities, and chooses one of the possible events randomly, weighted according to their probabilities. The Monte Carlo approach gives better transient and dynamic characteristics of SET circuits because its model the underlying microscopic physics. Tunnel events are modelled as discrete events as long as the electrons are confined on quantum dots.

2.3. Single-Electron Transistor (SET)

Single-electron Transistor is a Nanoelectronic device that used to monitor the electron tunnelling through the quantum island. SET consists of two tunnel junctions and a quantum island (quantum dot) about one nanometer range. The device structure just like MOS transistor, two junctions, as source and drain, instead of channel region the electrons can pass through the quantum island when reaches the coulomb energy. The effect of controlling the electron tunnel is coulomb blockade. The device can transfer the electrons from source to drain one by one under the application of gate voltage. So the tunnelling current is monitored by the voltage applied to the gate through a capacitor. This way charge carrier can transfer across the quantum island only after the sufficient voltage across the capacitor. Electron tunnelling rate based on the stochastic nature of the process takes place across the SET [15].

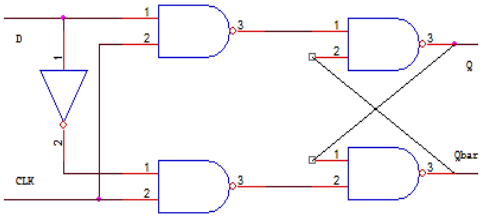


(a) (b) (c)

Fig. 1: (a) Schematic diagram for a tunnel junction, (b) Quantum dot island with two tunnel junctions, (c) Circuit diagram of the Single Electron Transistor.

3.a) Design of D-Flip-flop using Logic gates

The flip-flop is a basic circuit to store state information from two stable states. It is the basic storage element in the sequential logic systems. The design of D-Flip flop circuit using Logic gates is shown in Fig. 2. This circuit is a memory element with two inputs of different logical combination input values. The D-FF consists of 4 NAND gates and one NOT gate, it consists of different logic function.



Clock	D	Q
0	x	No Change
1	0	0
1	1	1

(a) (b)

Fig. 2: (a) Diagram of the D-flip flop using Logic gates (b) Logic table.

b) Design of D-Flip-flop using SET

The D-Flip flop circuit design using single electron transistor is shown in Fig.3. Hence the circuit comprises thirteen islands, N1 to N13, bounded by eight tunnel junctions. The capacitance of each junction and their resistances are shown in Table 1. The circuit also comprises 7 capacitors, and the values of different for varying nodes. The two voltage sources V_{dd} are constant and its value is 0.16V. The input voltage and clock are applied to the D and Clock respectively through the capacitors C.

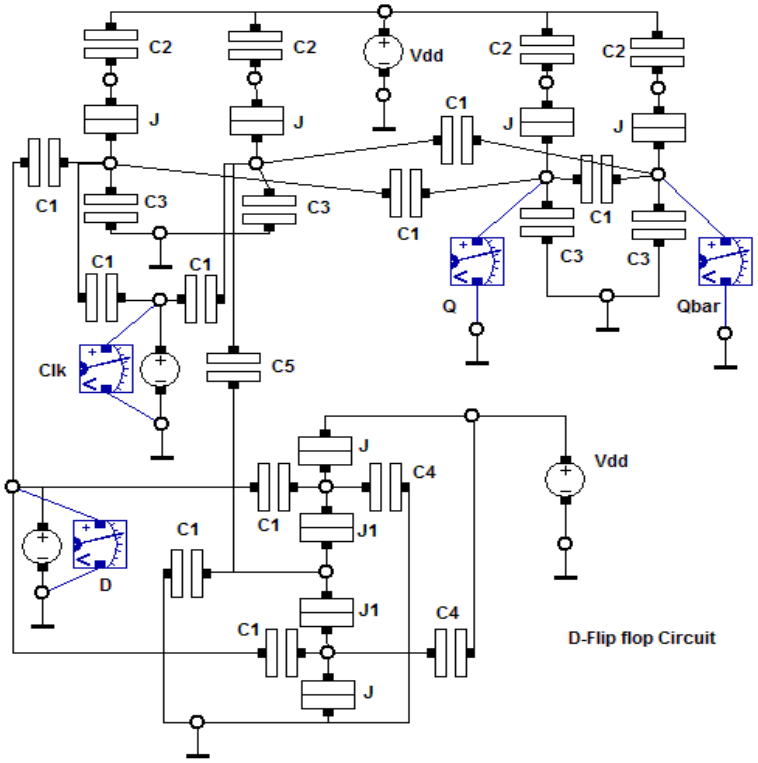


Fig. 3: Circuit diagram of single-electron D Flip flop

The input voltage and Clock, shown in Fig. 3, are the inputs of the D-Flip flop named as D and Clk, and it takes only two values 0.0V which tends to the logic ‘‘1’’, and -0.1V which tends to the logic ‘‘0’’. The output signals of the D-Flip flop are taken from islands nodes named Q and Qbar respectively.

Table 1: Resistance and Capacitance values of Tunnel Junctions.

Capacitance(F)	**Tunnel Junction(C,R)**	
$C1=5x10^{-18}$	J	$Cj=1x10^{-19}$
$C2=11.7x10^{-18}$		
$C3=9x10^{-18}$	J1	$Cj1=5x10^{-18}$
$C4=4.25x10^{-18}$		
$C5=1x10^{-18}$	$R=1x10^{5}$	

4. Analysis of Single-Electron D-Flip flop and Result

The single-electron D-Flip flop needs to be analysed the operational characteristics. From the corresponding output islands we take the outputs Q and Qbar respectively. The presence of zero voltage in the output islands corresponds to logic 1, whereas -0.1V voltage corresponds to logic 0. Hence, the input–output signals, of this D-Flip flop is shown in Fig.4. The two inputs are D and clock and the two outputs Q and Qbar respectively.

When the input vector [00] is applied an excess electron is transported via tunnelling to island nodes and the island output voltage at Q and Qbar becomes 0.1V. When the input

vector and the clock signal are high, the electron tunnels out of nodes are charged according to the figure- 4 given below.

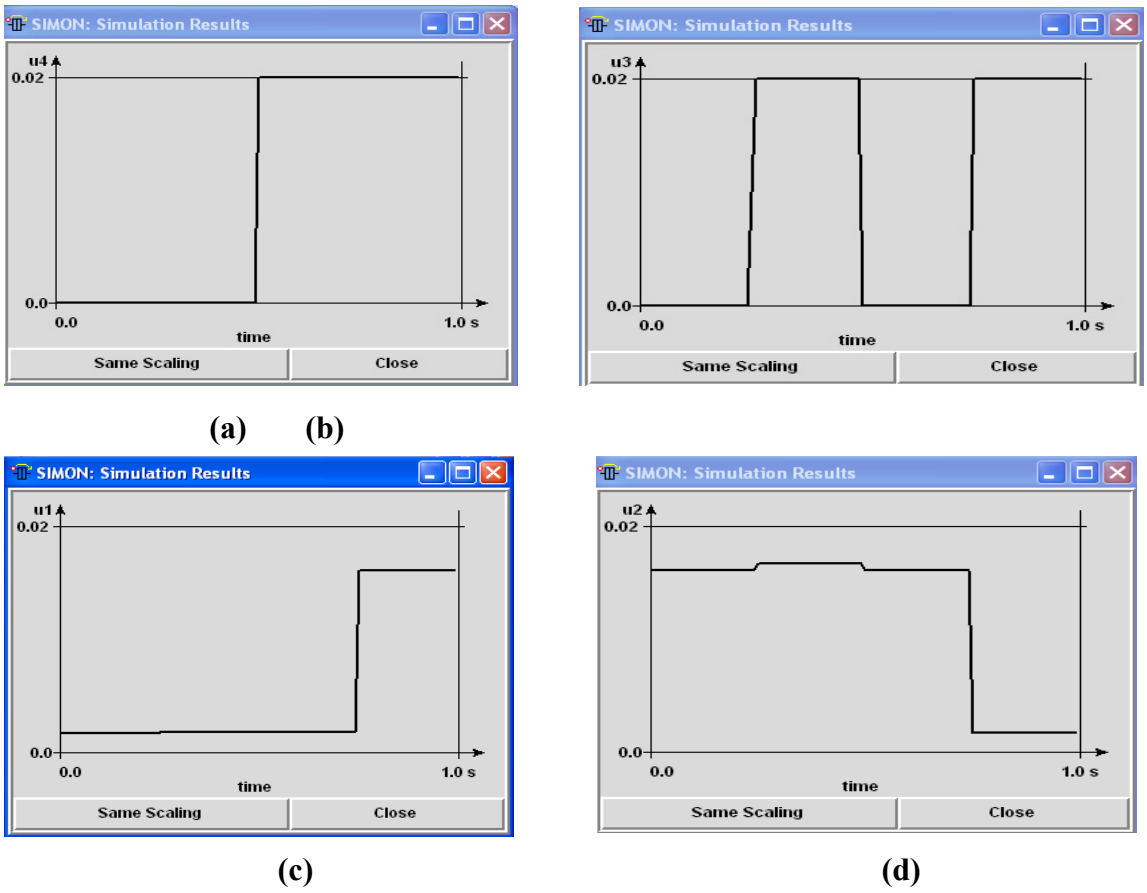
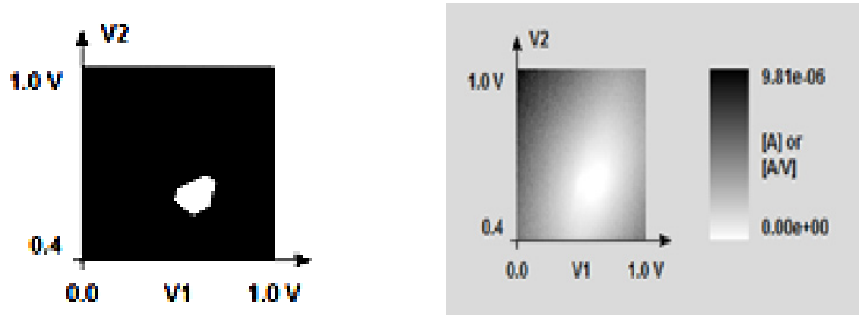


Fig. 4: Operation of the single-electron D Flip flop (a) time variation of the input clock CLK; (b) time variation of the input voltage V, (c) time variation of the output charge Q and (d) time variation of the output charge Q-bar.

To confirm the stable operation of flip flop, its stability plot was constructed using SIMON. This plot is shown in Fig. 5.White regions correspond to completely stable state operation with an integer number of excess or missing electrons on the islands, whereas black regions correspond to completely unstable state operation. The gray regions correspond to less stable regions. The darker the gray region, the more unstable the gate operation. The slight instability in gate operation is apparent in Fig. 5, where slight charge fluctuations are observed.



(a) **(b)**

Fig. 5: The stability plots of the single-electron D Flip flop.(a)

5. Conclusions

A single-electron D Flip flop was presented in this paper. This circuit produces their Q and Q-bar. The circuit comprises 8 tunnel junctions, seven capacitors and thirteen islands. Each output is through the island and the presence of positive charge on it corresponds to the logic '1', whereas the absence of charge corresponds to the logic '0'. The energy history diagrams were plotted. The simulation procedure and the operational characteristics were verified. The circuit allowed less delay time, and power consumption reduction.

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